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**Patent**

**Inventor(s):** Ralph Bonomo  
Daryl Cromer  
Joseph Pennisi

## **METHOD AND SYSTEM FOR INCREASING CONTROL INFORMATION FROM GPIOs**

### **FIELD OF THE INVENTION**

The present invention relates to general purpose input/output mechanisms (GPIOs), and more particularly to increasing control information from single GPIOs.

### **BACKGROUND OF THE INVENTION**

A trend emerging in computer system development and manufacturing involves a move toward a building block-based approach, where a system is created by a collection of building blocks. This approach places increasing need on the ability to detect, enable/disable, and customize building blocks to create the desired personality of the system.

The flexibility of varying the system configuration through building blocks requires that the POST (power-on self test) of the planar be able to detect, enable/disable, and configure the

various options installed. This is frequently handled with the use of General Purpose Input Outputs (GPIOs). Typically, a GPIO can only detect two states (high/low) and is dedicated to a function or a particular device. For example, if a particular card is installed, the GPIO may detect a low state, while if the card is not installed, the GPIO may detect a high state.

5           The push to a building block model is rapidly increasing the need for GPIOs to assist in the detection of the building blocks installed. However, some systems have to limit the number of GPIOs due to other design considerations. Thus, a need exists for a manner of increasing the amount of control information from GPIOs without increasing the number of GPIOs.

          The present invention addresses such a need.

## 10           **SUMMARY OF THE INVENTION**

          Aspects for increasing control information from a single general purpose input/output (GPIO) mechanism are described. The aspects include utilizing a single GPIO mechanism with a socket on a computer system. Determinations of whether a first card, a second card, or no card is installed in the socket occur according to detected changes in signal states on a single signal line between the GPIO mechanism and the socket. Detection of a first state on the single signal line indicates presence of a first card in the socket, while detection of a second state on the single signal line indicates presence of a second card in the socket. Detection of a state change on the single signal line indicates no card presence in the socket, where the changes occur in response to signals sent by a POST to the GPIO mechanism.

20           Through the present invention, an increase in the amount of control/information that is available using GPIOs is achieved in a straightforward and effective manner without increasing the number of GPIOs. Further, trinary states on a single signal line are detectable quite readily with

the inclusion of an R-C circuit on the single signal line. These and other advantages of the aspects of the present invention will be more fully understood in conjunction with the following detailed description and accompanying drawings.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

Figure 1 illustrates a block diagram of a portion of a computer system planar with a GPIO (general purpose input/output) in accordance with the present invention.

Figure 2 illustrates a block flow diagram of a method that achieves the ability to increase the control information provided by a single GPIO in accordance with the present invention.

## **DETAILED DESCRIPTION**

The present invention relates to increasing control information of single general purpose input/outputs (GPIOs). The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

Referring now to Figure 1, a block diagram of a portion of a planar is illustrated and includes a controller 10 which contains a GPIO 12. The GPIO 12 is coupled to a socket 14. As an exemplary embodiment of the functionality of the present invention, suppose the planar supports two different daughter cards, e.g., daughter card 1, daughter card 2, where daughter card 1 and daughter card 2 contain the same chips with minor changes in discrete logic. Thus, the

POST needs to know the status of card installation in socket 14, i.e., whether daughter 1, daughter 2, or no card is installed.

Under traditional operations, GPIOs follow Boolean logic (e.g., 0-low, 1-high) which allows for two states (True/False). Thus, the ability to detect three card states, i.e., whether a first card, a second card, or no card is installed, would require two GPIOs. A first GPIO, e.g., GPIO1, would be connected to a detect pin on daughter card 1, with the installed daughter card 1 grounding the detect pin. A second GPIO, e.g., GPIO2, would be connected to a detect pin on daughter card 2, with the installed daughter card 2 grounding that detect pin. When a POST routine of a controller reads the first and second GPIOs, a low for GPIO1 indicates that the first card is installed, a low on GPIO2 indicates that the second card is installed, and a high for both GPIO1 and GPIO2 indicates that no card is installed.

In contrast to the traditional operation requiring the use of two GPIOs for detection of three separate states, in accordance with the present invention, a third logical state (changeable) is created for a single GPIO, which is used to relay information. The changeable state is created with an R-C (resistor-capacitor circuit) on the GPIO to create a transient storage that allows POST to alter the state of the GPIO, as described in further detail hereinbelow. By way of example, the R-C circuit includes resistor 16, e.g., 500meg ohms, and capacitor 18, e.g., 200 micro farads, as the transient storage mechanism.

Figure 2 illustrates a flow chart of a method that achieves the ability one skilled in the art can adjust values to meeting timing requirements to increase the control information provided by a single GPIO, such as to detect installation of either of two card types or installation of no card, in accordance with the present invention. The process includes establishing a logic state associated

with installation of each card (step 20). For example, when the GPIO 12 is connected to a detect pin on daughter card 1, daughter card 1 grounds the detect pin (logic low state) when installed in socket 14, while when the GPIO 12 is connected to a detect pin on daughter card 2, daughter card 2 pulls-up the detect pin (logic high state) when installed in socket 14. POST then performs reads and writes to determine if GPIO 12 is state changeable. Thus, POST writes GPIO 12 with a first logic level signal, e.g., a low signal (step 22) and then reads GPIO 12 (step 24). POST writes GPIO 12 with a second logic level signal, opposite to the first logic level signal, e.g., a high signal (step 26). POST again reads GPIO 12 (step 28). The card installation status is then determined by POST (step 30), where if the GPIO 12 is changeable, then no card is installed, if GPIO 12 is low, daughter card 1 is installed, and if GPIO 12 is high, daughter card 2 is installed.

The ability to detect these three states via the single GPIO relies on the fact that the GPIO is held low (pull-down) or held high (pull-up) by the daughter card installed, regardless of whether POST writes a Low/High, because when a device is installed the pull-up/pull-down will dominate. Thus, when POST reads the GPIO, the GPIO will always indicate the value forced by the pull up/down of the card type installed. If the GPIO is state changeable, when there is not a pull-up/pull-down due to the presence of a device in the socket, then POST will be able to read what was written. In this manner, three information states are able to be determined from a single signal line.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. For example, the same approach could be used for jumper pins to provide configuration



## CLAIMS

What is claimed is:

- 1           1. A method for increasing control information from a single general purpose  
2 input/output (GPIO) mechanism, the method comprising:  
3           utilizing a single GPIO mechanism with a socket on a computer system; and  
4           determining whether a first card, a second card, or no card is installed in the socket  
5 according to detected changes in signal states on a single signal line between the GPIO  
1 mechanism and the socket.  
1           2. The method of claim 1 wherein determining further comprises writing a signal in a first  
2 state by a POST (power-on self test) routine to the GPIO mechanism.  
1           3. The method of claim 2 wherein determining further comprises reading a state of the  
2 GPIO mechanism by the POST routine.  
1           4. The method of claim 3 wherein determining further comprises writing the signal in a  
2 second state by the POST routine to the GPIO mechanism.  
1           5. The method of claim 4 further comprising reading a state of the GPIO mechanism by  
2 the POST routine.  
1           6. The method of claim 5 wherein when the state of the GPIO mechanism changes in  
2 accordance with state changes by the POST routine, no card is installed in the socket.  
1           7. The method of claim 6 wherein when the state of the GPIO mechanism does not  
2 change, one of the first and second cards is installed.  
3



1 8. The method of claim 7 wherein one of the first and second cards pulls-up the signal  
2 line, and the other of the first and second cards pulls-down the single signal line.

1 9. The method of claim 1 wherein the first and second cards comprise first and second  
2 POV cards.

1 10. A system for increasing control information from a single general purpose  
2 input/output (GPIO) mechanism, the system comprising:

3 a computer system planar including a socket; and

4 a GPIO means coupled to the socket via a single signal line, wherein at least three states of  
1 occupancy of the socket is detected according to state changes on the single signal line.

1 11. The system of claim 10 wherein when a first card occupies the socket, the single  
2 signal line is pulled to a first logic state.

1 12. The system of claim 11 wherein when a second card occupies the socket, the single  
2 signal line is pulled to a second logic state.

1 13. The system of claim 12 wherein when no card occupies the socket, the single signal  
2 line changes state in response to state changes of a signal from a POST (power-on self test)  
3 routine.

1 14. The system of claim 13 further comprising a controller coupled to the GPIO to  
2 perform the POST routine.

1 15. The system of claim 14 further comprising a transient storage circuit coupled to the  
2 single signal line to assist in the detection of state changes.

1 16. The system of claim 15 wherein the transient storage circuit comprises a resistor-  
2 capacitor (R-C) circuit.



## ABSTRACT

Aspects for increasing control information from a single general purpose input/output (GPIO) mechanism are described. The aspects include utilizing a single GPIO mechanism with a socket on a computer system. Determinations of whether a first card, a second card, or no card is installed in the socket occur according to detected changes in signal states on a single signal line between the GPIO mechanism and the socket. Detection of a first state on the single signal line indicates presence of a first card in the socket, while detection of a second state on the single signal line indicates presence of a second card in the socket. Detection of a state change on the single signal line indicates no card presence in the socket, where the changes occur in response to signals sent by a POST (power-on self test) routine to the GPIO mechanism.

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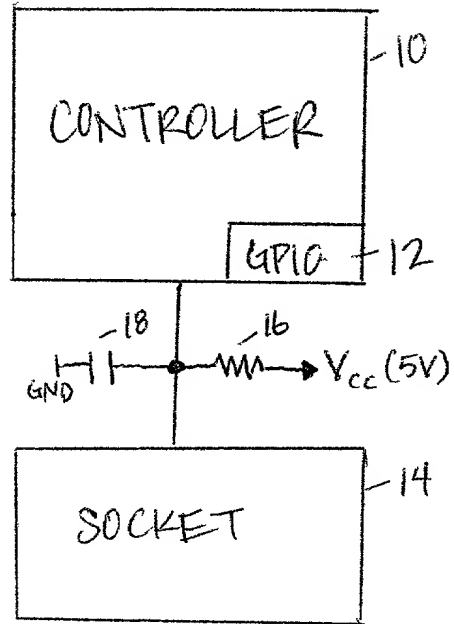


FIGURE 1

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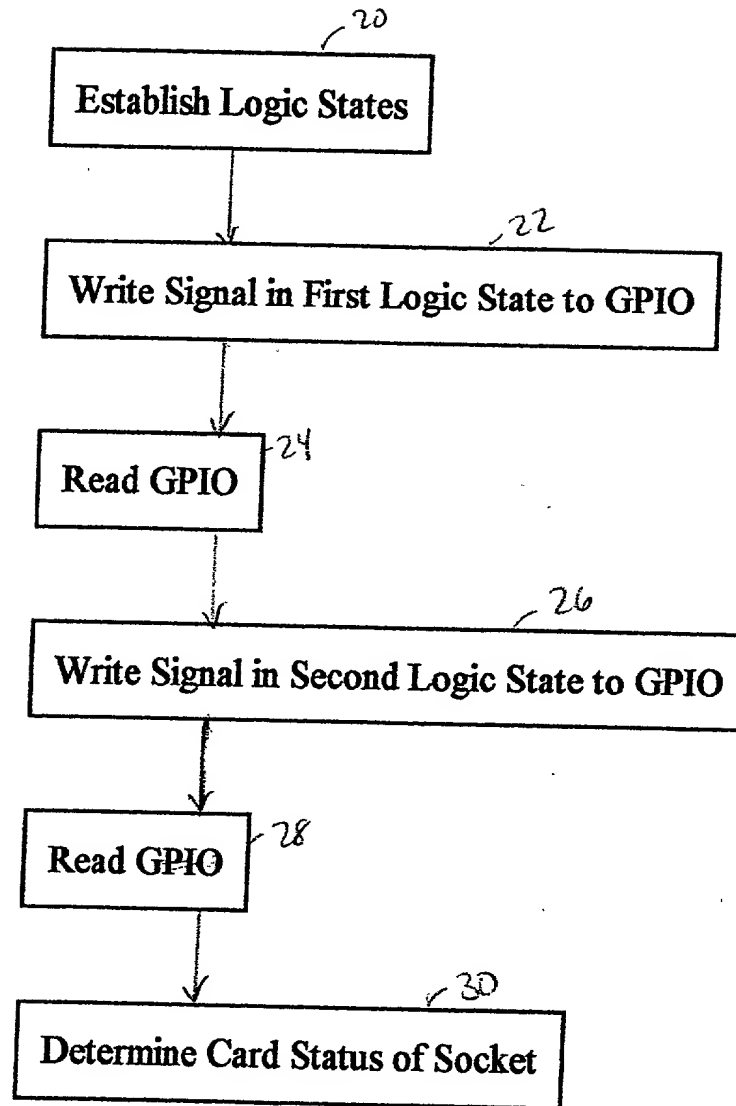


FIG. 2